## REMARKS

The following is intended as a full and complete response to the Office Action dated December 8, 2008, having a shortened statutory period for response set to expire on March 8, 2009. The Examiner rejected claims 1, 6, 8, 10, 12, and 15-21 under 35 U.S.C. §103(a) as being unpatentable over Wolrich (U.S. 6,694,380) in view of Nishihara (U.S. 2001/0010074). The Examiner rejected claim 5 under 35 U.S.C. §103(a) as being unpatentable over Wolrich and Nishihara in further view of Shukla (U.S. 2002/0042875). The Examiner rejected claim 7 under 35 U.S.C. §103(a) as being unpatentable over Wolrich and Nishihara in further view of Warren (U.S. 6,675,284). The Examiner rejected claim 9 under 35 U.S.C. §103(a) as being unpatentable over Wolrich and Nishihara in further view of Kean (U.S. 5,469,003). The Examiner rejected claim 11 under 35 U.S.C. §103(a) as being unpatentable over Wolrich and Nishihara in further view of Pham (U.S. 2003/0074473). The Examiner rejected claims 13-14 under 35 U.S.C. §103(a) as being unpatentable over Wolrich and Nishihara in further view of Schunk (U.S. 6,980,515). These rejections are respectfully traversed.

Claim 1 is amended to recite the limitations of a plurality of nodes, where each node included in the plurality has a fixed and different architecture that corresponds to a particular algorithmic function. Further, each node is coupled to one or more other nodes in the plurality of nodes via a programmable interconnection network. Claim 1 is further amended to recite the limitations of a reconfigurable input/output (I/O) controller coupled to a first node in the plurality of nodes via the programmable interconnection network. Support for these amendments can be found at, among other places, paragraphs [0019]-[0021] and Figure 1 of the present application. The cited references fail to teach or suggest these limitations.

The Examiner concedes that Wolrich does not disclose the limitations of a reconfigurable I/O controller coupled via the programmable interconnection network to the plurality of nodes, as recited in amended claim 1. Instead, the Examiner relies on Nishihara for teaching these limitations. Nishihara discloses, at Figure 19A, a typical field programmable gate array (FPGA) programmable logic circuit sector, and discloses, at Figure 19B, a typical complex programmable logic device (CPLD) programmable logic circuit sector. As is generally known to those having ordinary skill in the art, the

logic cells that make up an FPGA or a CPLD are programmable and/or configurable. Importantly, each of the logic cells in the FPGA disclosed in Nishihara has an identical architecture to the other logic cells in the FPGA. Similarly, each of the logic cells in the CPLD has an identical architecture to the other logic cells in the CPLD. Accordingly, Nishihara fails to teach or suggest the limitations of each of the nodes in the plurality of nodes having a fixed and different architecture that corresponds to a particular algorithmic function, as expressly recited in amended claim 1.

As the foregoing illustrates, neither Wolrich nor Nishihara teaches or suggests each and every limitation of amended claim 1. Therefore, no combination of these references can render claim 1 obvious. For these reasons, Applicants submit that claim 1 is allowable. The remaining claims depend from allowable claim 1 and therefore are also allowable.

## CONCLUSION

Based on the above remarks, Applicants believe that they have overcome all of the objections and rejections set forth in the Office Action mailed December 8, 2008 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicant's undersigned representative at the number provided below.

Respectfully submitted,

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